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Exploiting Fine Grained Parallelism in SPE

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Table of contents

Introduction

Fundamental Problem

- RAM does not capture memory access complexity
- Computational complexity is not enough on actual machines

Strategy

- Machine models (memory and processor)
- Algorithmic techniques

Questions

- What can be imported from other settings/contexts?
- Is it possible/convenient to exploit parallelism in a scalar setting?

Models and Algorithms

Two major strategies to cope with latency:

- Temporal/Spatial Locality
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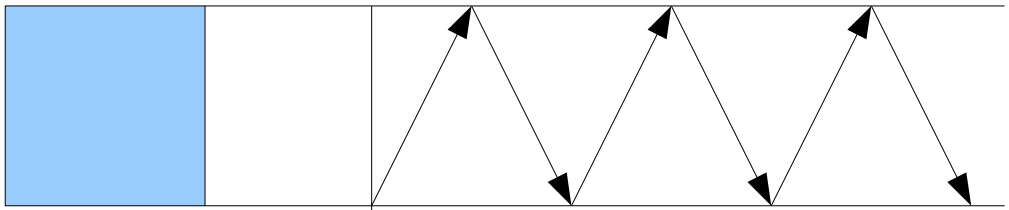
Models and Algorithms

Two major strategies to cope with latency:

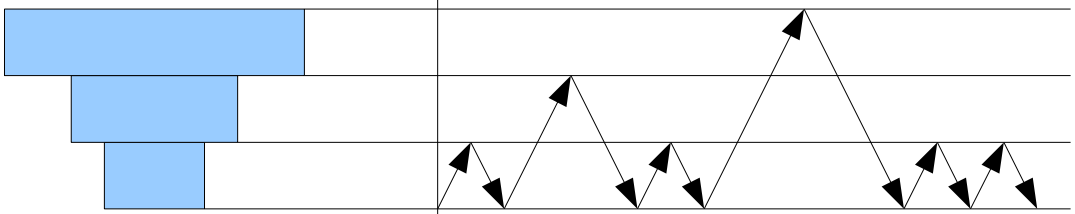
- Temporal/Spatial Locality
  $\Rightarrow$ Hierarchical Memories, Block Transfer
  $\Rightarrow$ Memory access function $a(x)$
- Concurrency
  $\Rightarrow$ Pipelined Memories
  $\Rightarrow$ Constant access request rate

Memory Models

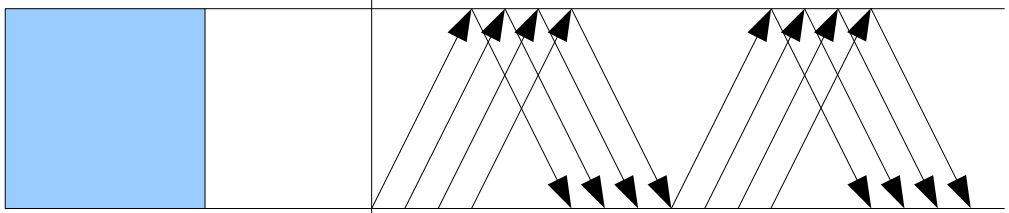
RAM with latency



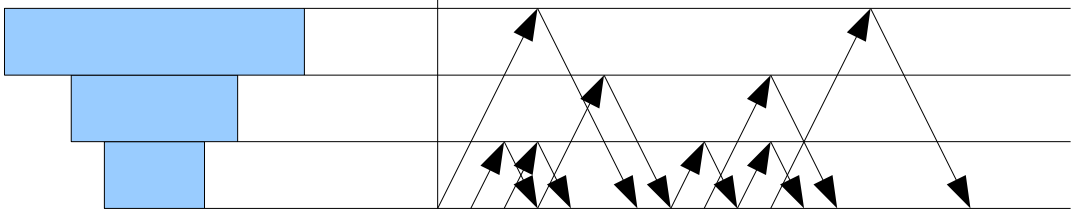
Hierarchical Memory



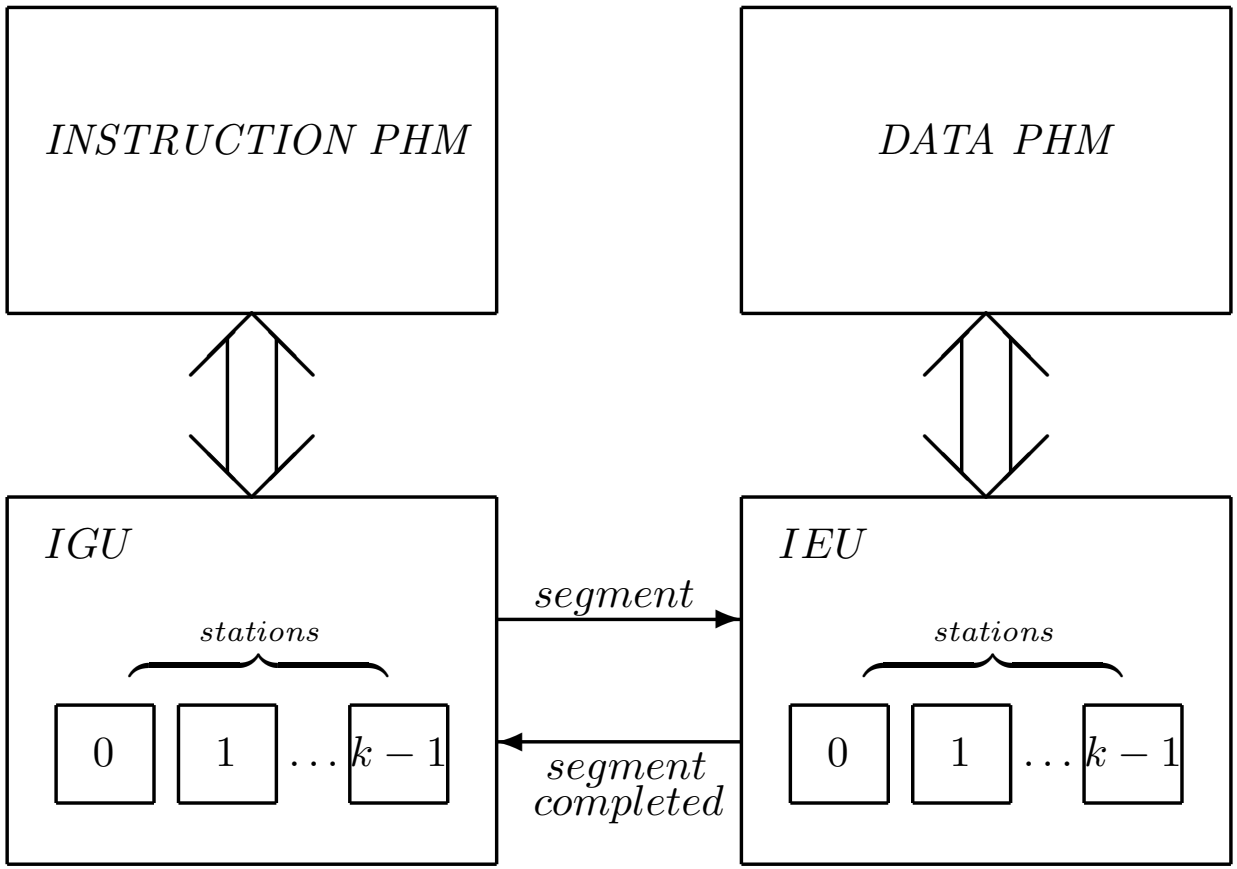
Pipelined Memory



Pipelined Hierarchical Memory



Speculative Prefetcher and Evaluator



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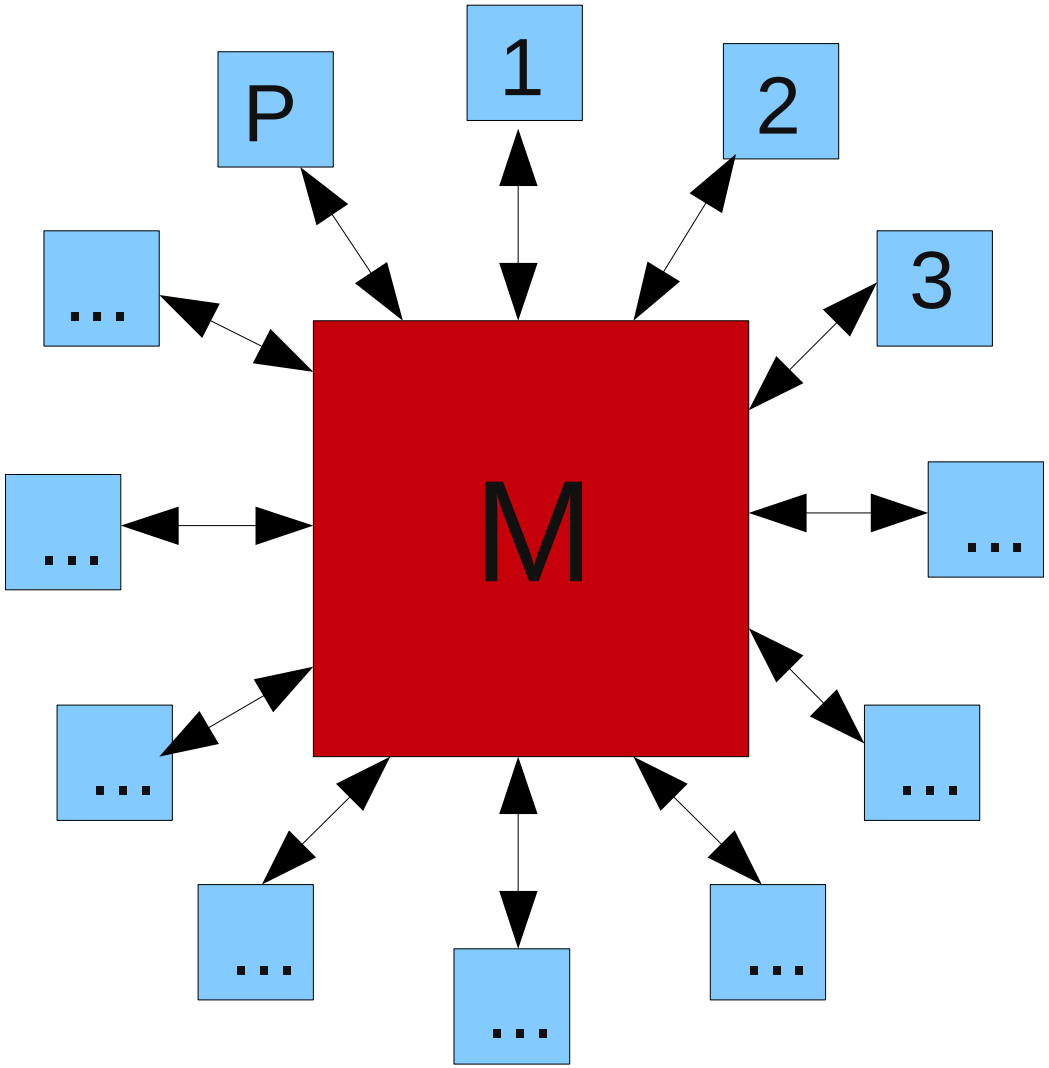
- ...or even $O(1)$ address dependence depth
- Enhancements such as dynamic loop unrolling and branch prediction are allowed

Parallel Random Access Machine



Parallel Random Access Machine

Many equivalent flavours: SIMD, MIMD...

The actual difference is in how shared memory is managed:

- EREW: exclusive read, exclusive write
- CREW: concurrent read, exclusive write
- CRCW: concurrent read, concurrent write (contention policy)

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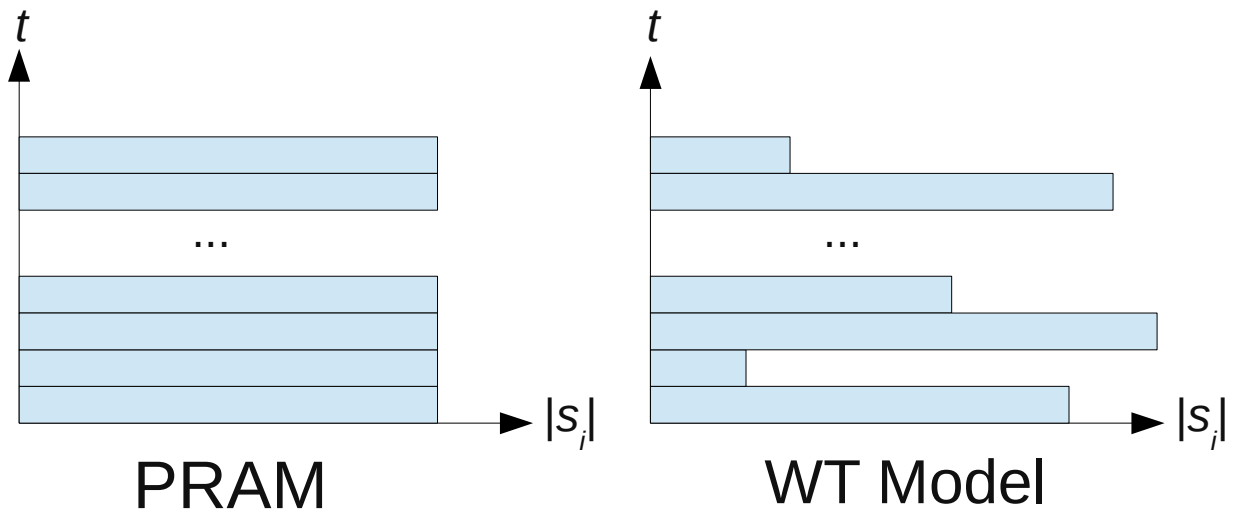
- Time T; Work $W = \sum_{i=1}^{T} p_i$
- Easily schedulable on PRAM: $O(W/P + T)$



Exploiting Parallelism

- PRAM to Disk Model

  Chiang, Y., Goodrich, M. T., Grove, E. F., Tamassia, R., Vengroff, D. E., Vitter, J. S.: External-Memory Graph Algorithms. SODA '95
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- PRAM to Pipelined Memory

  Luccio, F., and Pagli, L.: A model of sequential computation with pipelined access to memory. *Math. Syst. Theory 26*

Our Work

Our Work

- Parallel model: Work-Time Framework
- Sequential model: SPE
- A general technique for implementing WT Algorithms on SPE
- Large classes of optimal SPE programs

Novelty

- Explicitly refer to a feature of problems: available parallelism
- Target physically implementable machines, not bound to a particular memory access function

WT Simulation - Single Step

Simulation of parallel step i (exclusive write)

WT

for $j, 1 \leq j \leq p$ pardo
    operation$_j$

SPE

segmentsize(min(k, p))
for $j, 1 \leq j \leq p$ do
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- Program size: $O(1)$
- Δ Space: $O(p_i)$
- Time: $O(p + a(M^i_{SPE}))$

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- Memory accesses fully overlap

  $\Rightarrow$ proportional to p_i and $a(M^i_{SPE})$

WT Simulation - Concurrent Write

Different solutions, depending on the concurrent write policy:

- *priority* policy $\rightarrow$ predicated instructions
- associative op. policy $\rightarrow$ accumulation

`segmentsize(min(`k`, `p`))`
`for` $j, 1 \leq j \leq p$ `do`
`instructions`$_j$
$acc \leftarrow \max\{acc; output_j\}$

- Also an `if(test)` statement can be used...
  ...when the test is simple enough!

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Optimal SPE programs if

- Work–optimal WT algorithms
- The *average parallelism* is larger than worst case latency

Merge

Problem: merging 2 sorted lists of n elements.

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- $\Rightarrow T_{SPE} = O(W + T \cdot a(M)) = O(n + \log n \cdot a(n))$
- linear for $a(x) = x^{\alpha}, 0 < \alpha < 1$, $a(x) = \log x$.

On other hierarchical models:

- $O(n \log n)$ if $a(x) = x^{\alpha}, 0 < \alpha < 1$
- $O(n \log^* n)$ if $a(x) = \log x$

MergeSort

Problem: sorting a list of n elements.

Warning

Merge is linear *only if* the input is in the fastest $O(n)$ locations.

Solution

When merge istances are too small wrt latency, execute them in an interleaved fashion.

Non–local Matrix Multiplication

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Space complexity

$O(n^3)$ memory is required!

Conclusions and Future Work

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- Large memory footprint, if too much parallelism

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Future Work

- Integration with locality exploitation
- Exploitation of *coarse grained* parallelism (D-BSP)

Thank you!

Thank you for your attention!

. . . questions?